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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,870	06/21/2000	Charles S. Farlow	100.015US01	7541
34206	7590	11/29/2005	EXAMINER	
FOGG AND ASSOCIATES, LLC P.O. BOX 581339 MINNEAPOLIS, MN 55458-1339			ODOM, CURTIS B	
			ART UNIT	PAPER NUMBER
			2634	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. <span style="float: right;">OK</span> 09/598,870	Applicant(s) FARLOW, CHARLES S.	
	Examiner Curtis B. Odom	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.  
 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-6,8-32,35-41 and 43-51 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☒ Claim(s) 9-27 and 45-48 is/are allowed.  
 6) ☒ Claim(s) 1-6,8,28-32,35-41,43,44 and 49-51 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 18 June 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 8, 28-32, 35-41, 43, 44, and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (previously cited in Office Action 5/12/2005) in view of Coonce et al. (U. S. Patent No. 4, 064, 370).

Regarding claim 1, Ueda discloses an equalization circuit (Fig. 1), comprising:

- an input (Fig. 1, block 40) adapted to receive signals from a communications channel;
- a plurality of equalizer circuits (Fig. 1, blocks 41 and 42) coupled to the input and operable to generate a plurality of intermediate signals;
- a selector circuit (Fig. 1, block 48) responsive to the equalizer circuits that selects one of the intermediate signals; and
- an output (Fig. 1, output of block 48) coupled to the selector circuit that receives the selected intermediate signal.

Ueda does not disclose a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for a selected period of time.

Coonce et al. discloses a plurality of buffer circuits (Fig. 1, block 205, column 3, line 62-column 4, line 24) which buffer intermediate signals for a plurality of time (duration of a time slot). Coonce et al. discloses that synchronism throughout the device can be controlled by controlling the timing of the buffers (column 8, lines 8-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each equalization data path in sequence (Coonce et al., column 4, lines 62-64) and maintain synchronization between the data paths.

Regarding claim 2, which inherits the limitations of claim 1, Ueda et al. discloses the equalizer circuits comprise one of a fixed and adaptive equalizer (column 19, line 65-column 21, line 17).

Regarding claim 3, which inherits the limitations of claim 2, Ueda et al. discloses the adaptive equalizers comprise one of a linear equalizer and a nonlinear equalizer (column 19, line 65-column 21, line 17).

Regarding claim 4, which inherits the limitations of claim 2, Ueda discloses each of the adaptive equalizers comprises one of a transversal structure and a lattice structure (column 9, lines 9-15).

Regarding claim 5, which inherits the limitations of claim 2, Ueda discloses each of the adaptive equalizers uses one of a recursive least squares algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm (column 25, lines 41-45).

Regarding claim 6, which inherits the limitations of claim 1, Ueda discloses the equalizer circuits provides a signals that reflects the relative quality (error values) of the intermediate signals from a plurality of equalizer circuits to the selector circuit to select the intermediate signal (column 20, line 61-column 21, line 17).

Regarding claim 8, which inherits the limitations of claim 1, Coonce discloses the buffer circuits buffer the intermediate signals for approximately the duration of a time slot of the communication channel column 3, line 62-column 4, line 24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the equalizer of Ueda with the teachings of Coonce et al. in order to process each equalization data path in sequence with regards to each time slot (Coonce et al., column 4, lines 62-64) and maintain synchronization between the equalization data paths.

Regarding claims 28-32, 35 and 36 Ueda and Coonce et al. discloses all the limitations of claims 28-32 (see rejection of claims 1, 6 and 8) including receiving the signal over a wireless communication channel (Fig. 11), loading selected coefficients (wherein the coefficients are selected during training mode) for a plurality of equalizers prior to receiving a signal over the communication channel (Ueda, column 2, line 65-column 4, line 41), and generating one of a mean squared error and a peak error over a selected (one burst) interval (Ueda, Fig. 1, blocks 45 and 45, column 20, lines 61-column 21, line 17) . Ueda does not disclose receiving the signal over a communication channel of a hybrid fiber coax network. However, it would have been obvious to one skilled in the art at the time the invention was made that the signal could have been received over a hybrid fiber coax network. Thus, transmitting a signal over a hybrid fiber coax network does not constitute patentability.

Regarding claims 37-41, Ueda and Coonce et al. disclose all the limitations of claims 37-41 (see rejections of claims 1, 6, 8, 29 and 30) including further processing the parallel outputs of the bank of adaptive equalizers (Ueda, Fig. 1, blocks 45 and 46), generating a quality measure of the output of each of the bank of equalizers (Ueda, Fig. 1, block 45 and 46, column 20, line 61-column 21, line 17), and selecting an output of one of the equalizer based on the quality measure (Ueda, column 21, line 1-26). Ueda further discloses the further processing comprises detecting errors at the packet level (column 21, lines 1-6, error values). Ueda and Coonce et al. do not disclose processing the parallel outputs comprises forward error correcting the parallel outputs. However, it would have been obvious to one skilled in the art at the time the invention was made to include this feature correct errors that may inhibit further signal processing. Forward error correction (FEC) is a well known method which aids in the recovery of the original data signal at the receiver. Thus, forward error correcting does not constitute patentability.

Regarding claims 43 and 44, the claimed apparatus includes features corresponding to the above rejection of claims 1 and 2 which is applicable hereto.

Regarding claims 49-51, Ueda and Coonce et al. disclose all the limitations of claims 49-51, (see rejections of claims 1, 29 and 30) including at least one base station to provide connection to a core network including a circuit that receives signals from the core network and provides the signal to a plurality of remote users over at least one communication channel, the base station further including a receiver that receives TDMA signal from a plurality of remote users over at least one communication channel (Fig. 11, column 1, lines 10-16).

*Allowable Subject Matter*

3. Claims 9-27 and 45-48 allowable over prior art references because related references do not disclose a plurality of equalizers coupled to a plurality of decoders forming multiple data paths, wherein one of data paths containing an equalizer/decoder is selected.

*Conclusion*

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Uesugi et al. (U. S. Patent No. 6, 347, 391) discloses selection one of a plurality of equalized signals based on an error measurement.

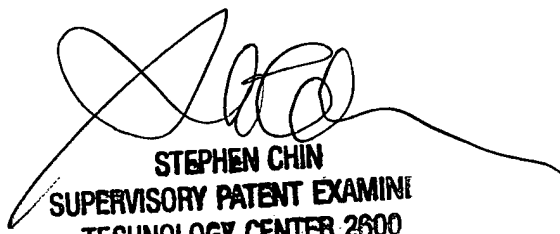
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2634

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom  
November 28, 2005



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